Ultra-Thin Body Self-Aligned InGaAs MOSFETs on Insulator (III-V-O-I) by a Tight-Pitch Process

Jianqiang Lin

Lukas Czornomaz*, Nicolas Daix*,

Dimitri A. Antoniadis, and Jesús A. del Alamo

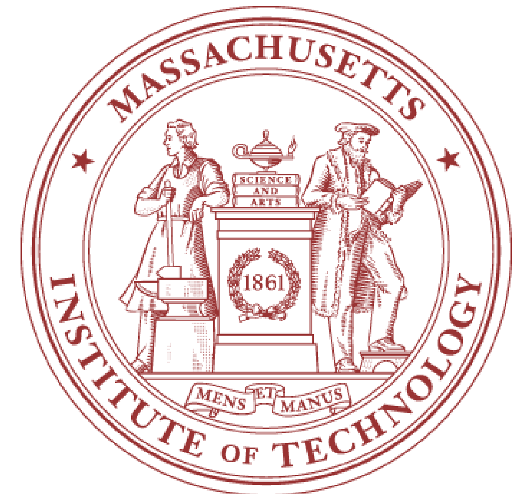
Microsystems Technology Laboratories, MIT

** IBM Zurich Research Laboratory*

June 22, 2014

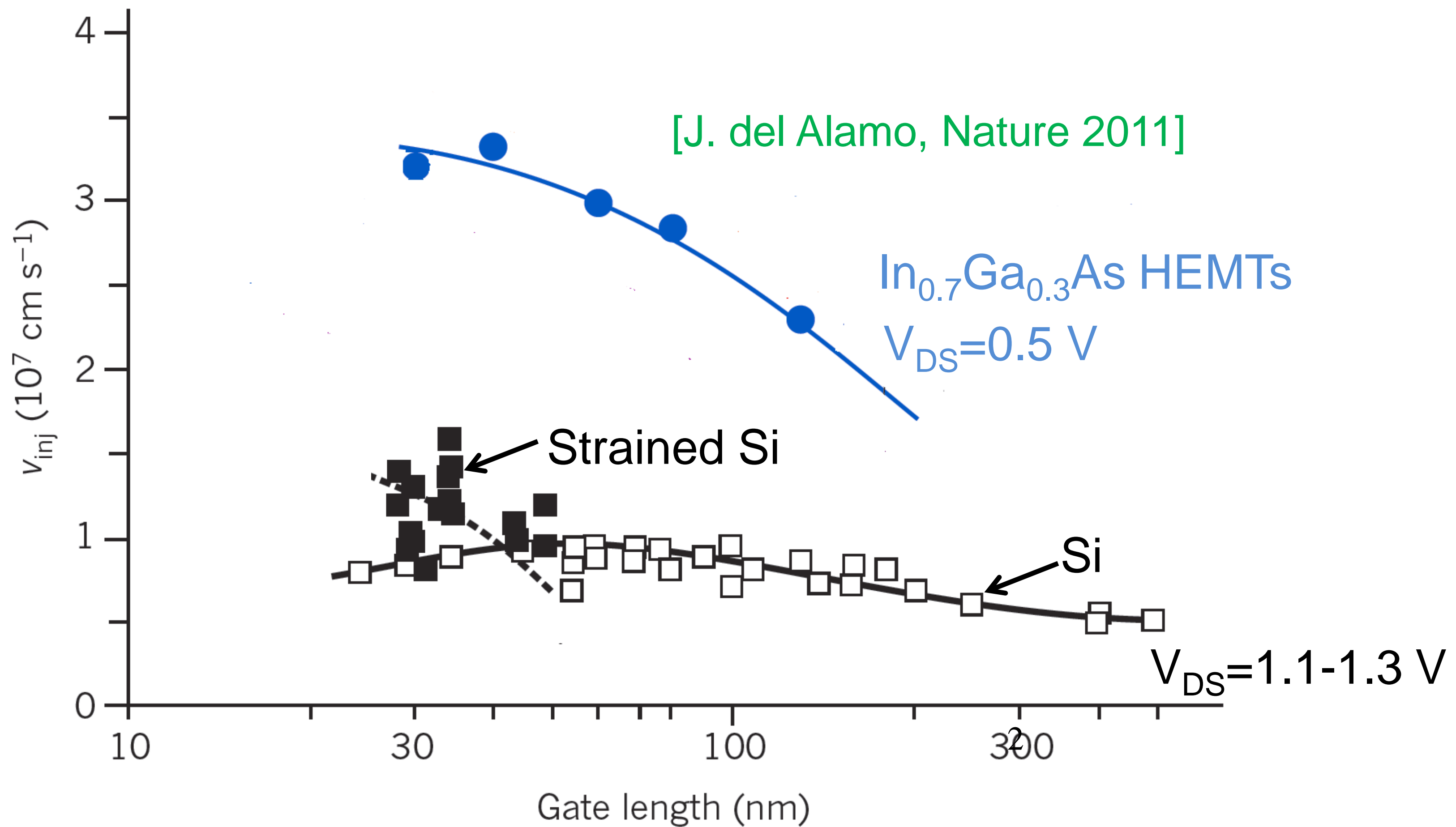
Sponsors:

- FCRP-MSD Center
- MIT Donner Chair
- MIT SMA and SMART programs
- Project Marie Curie FP7-PEOPLE-2011- IEF-300936 LATICE



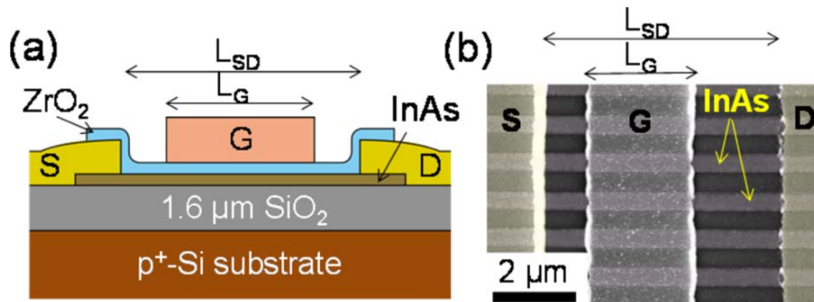
Motivation

- Superior electron transport properties in InGaAs channel

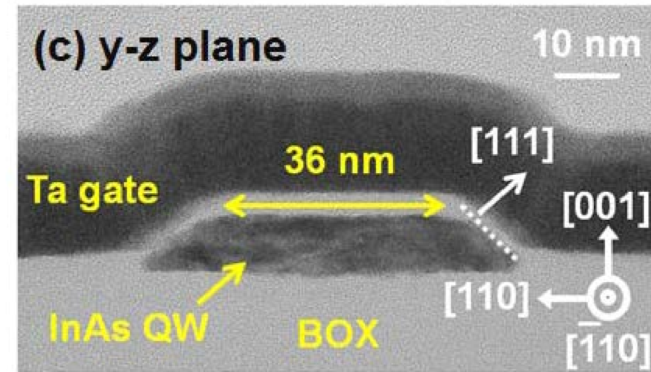


Si/III-V Integration

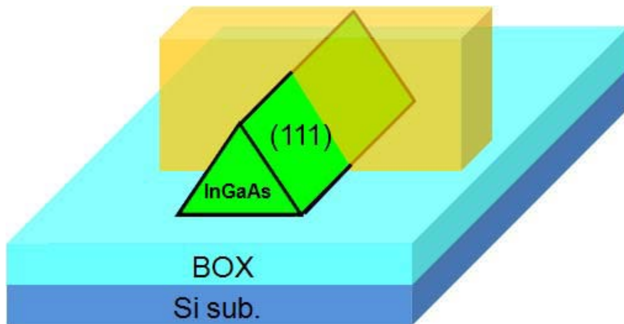
UC Berkeley [K. Takei, APL 2013]



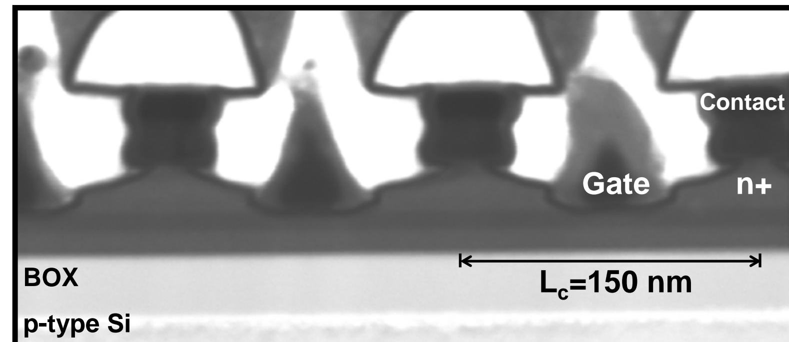
U Tokyo [S. Kim, IEDM 2013]



AIST [T. Irisawa, IEDM 2013]



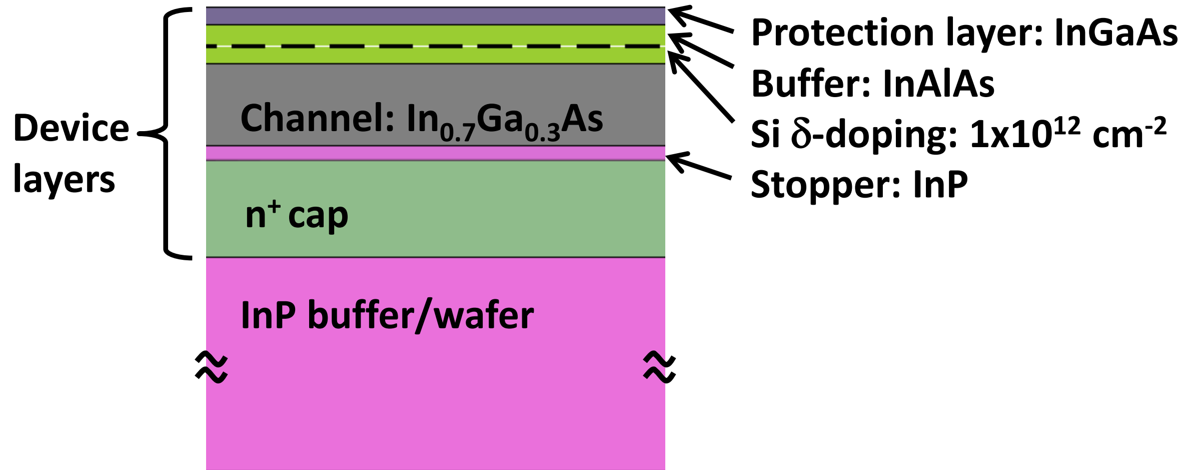
MIT / IBM [This work]



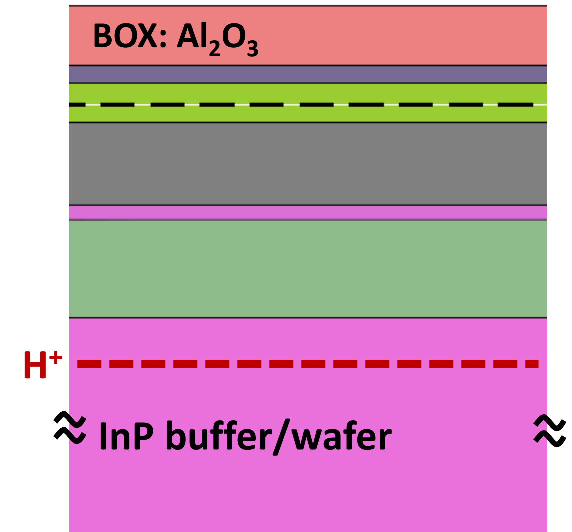
Substrate Fabrication

Following Czornomaz, IEDM 2012

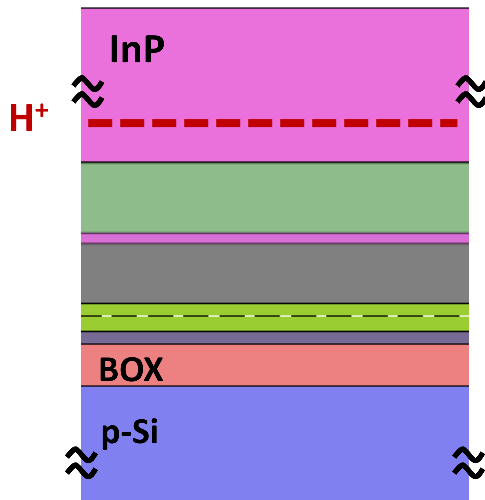
1. MBE growth



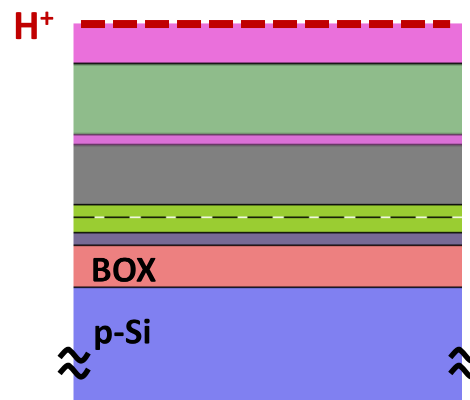
2. H^+ implants & Al_2O_3 depo



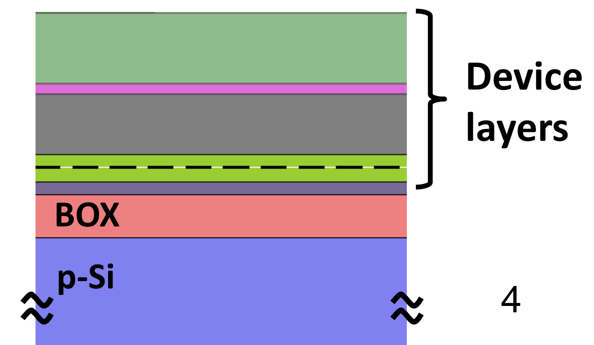
3. Wafer bonding



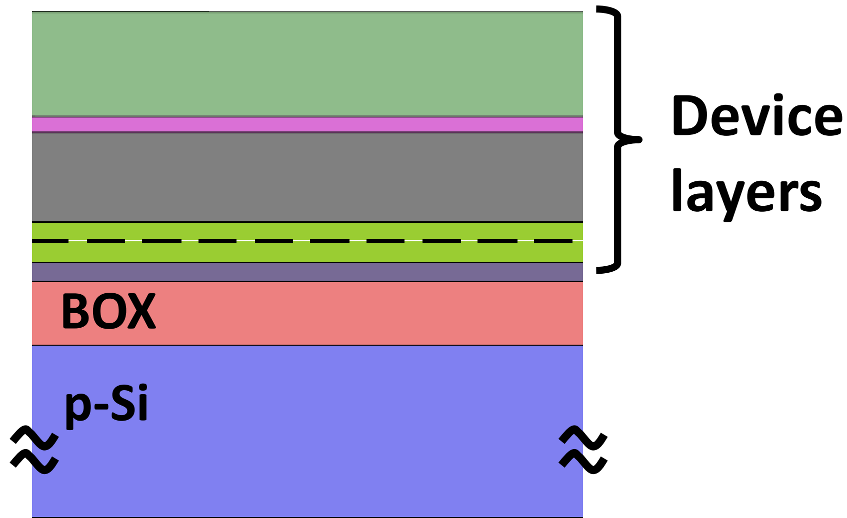
4. Thermal split

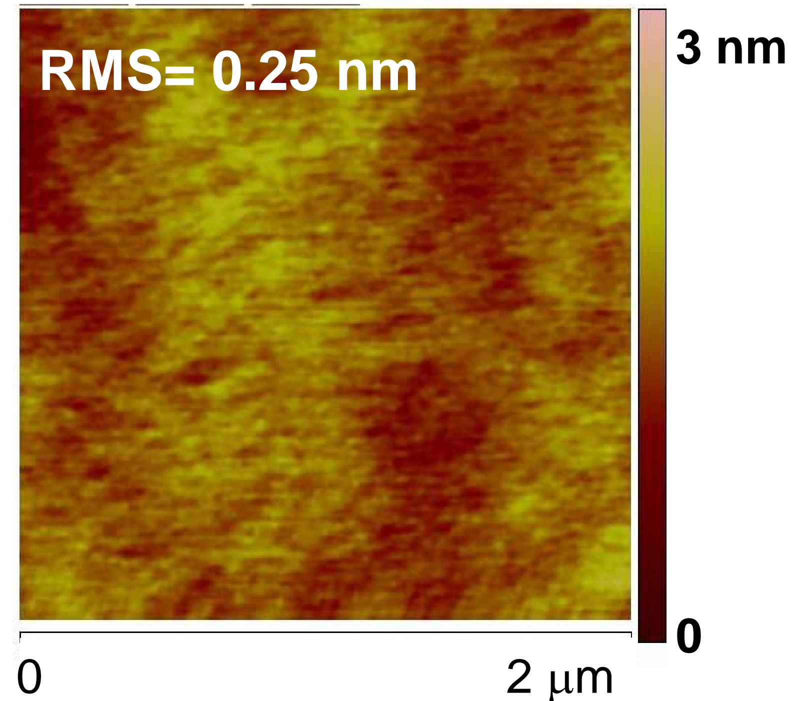


5. InP etch back



Substrate Fabrication



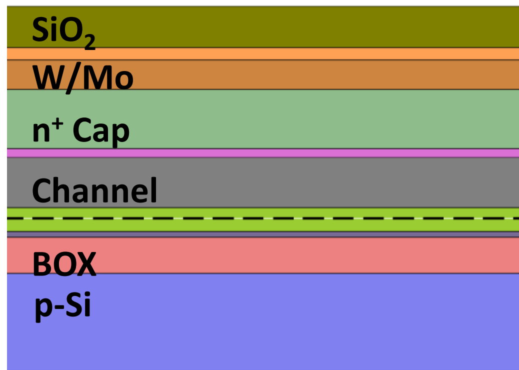


- Final substrate
- Smooth surface of final substrate

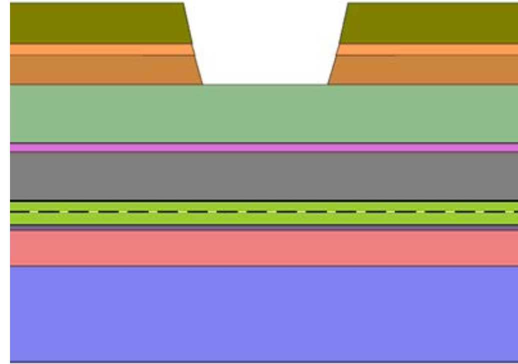
Device Fabrication

Following Lin, IEDM 2013

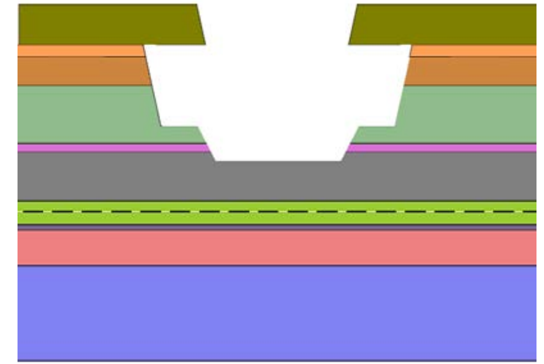
1. Ohmic/Oxide deposition



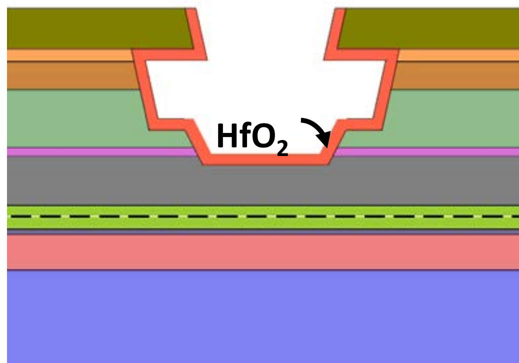
2. Gate opening, Mesa isolation



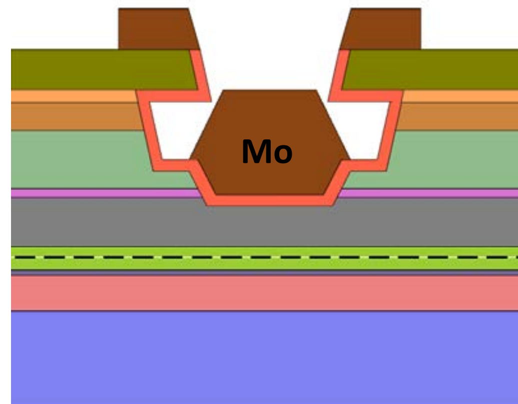
3. 3-step gate recess, Damage anneal



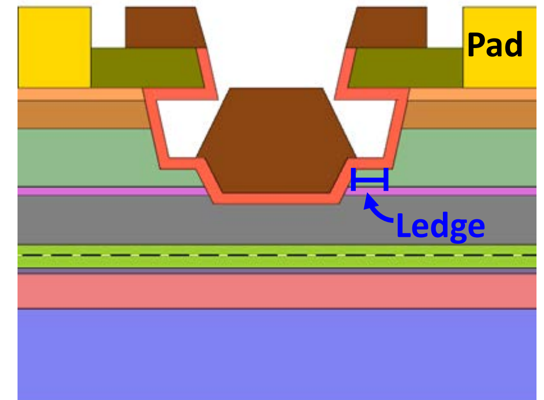
4. Gate oxide ALD



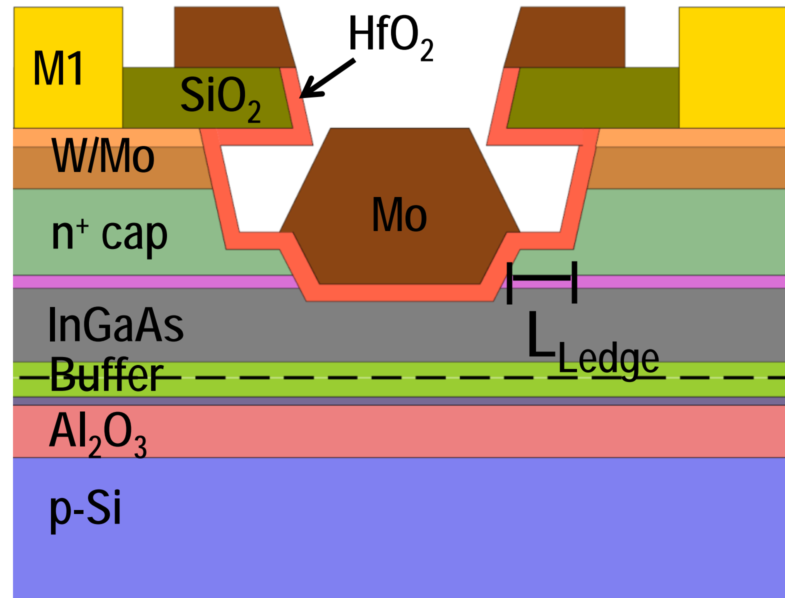
5. Gate metal



6. Pad formation

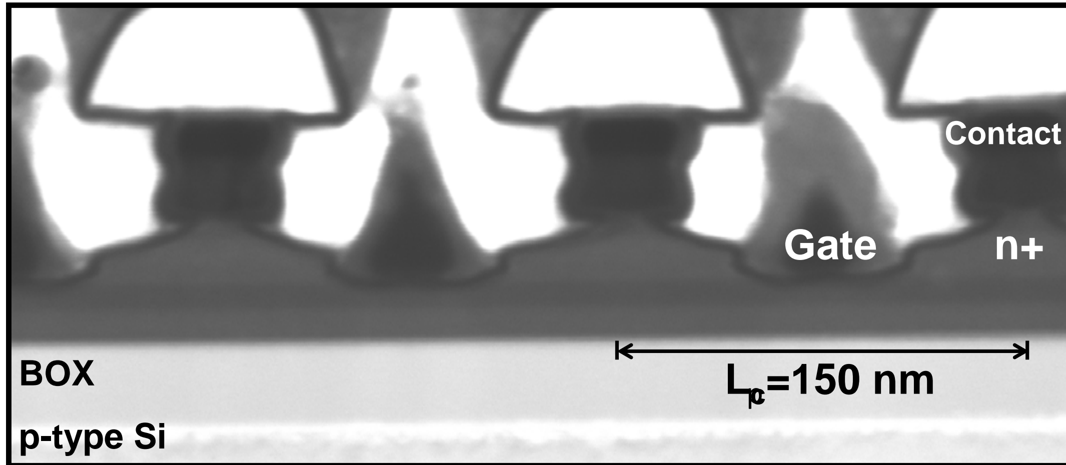


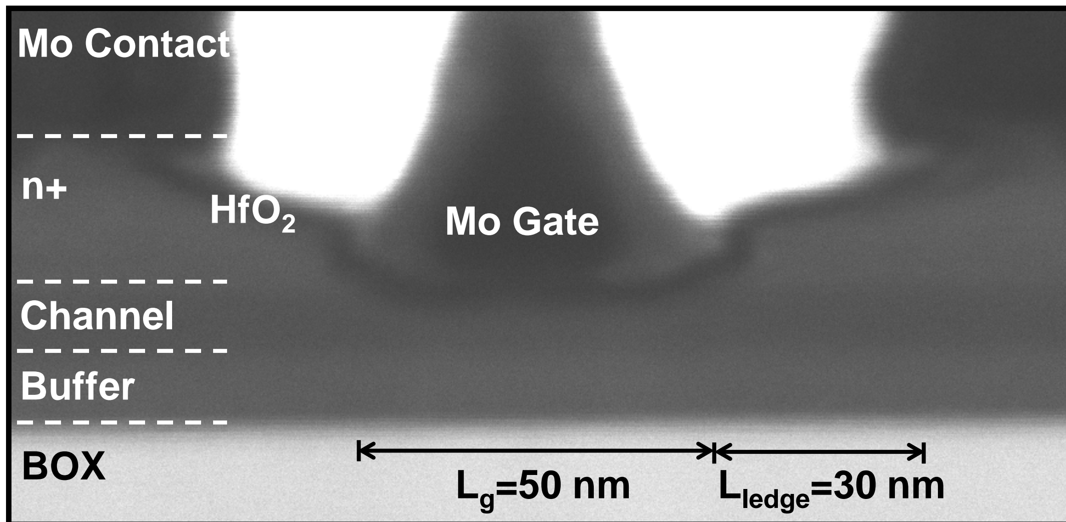
Final Device Structure



- Gate dielectric HfO_2=3.5 nm, EOT=0.7 nm
- Intrinsic channel $In_{0.7}Ga_{0.3}As$= 8 nm
- BOX Al_2O_3 = 30 nm

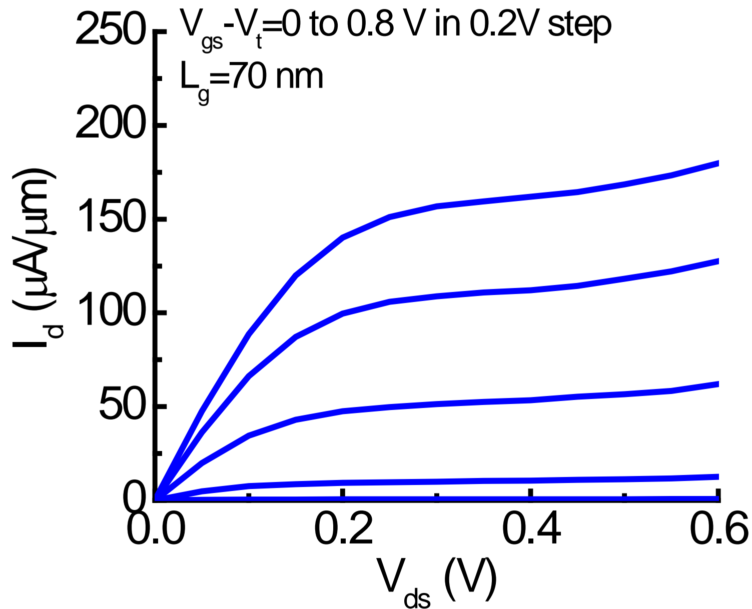
TEM Cross Sections

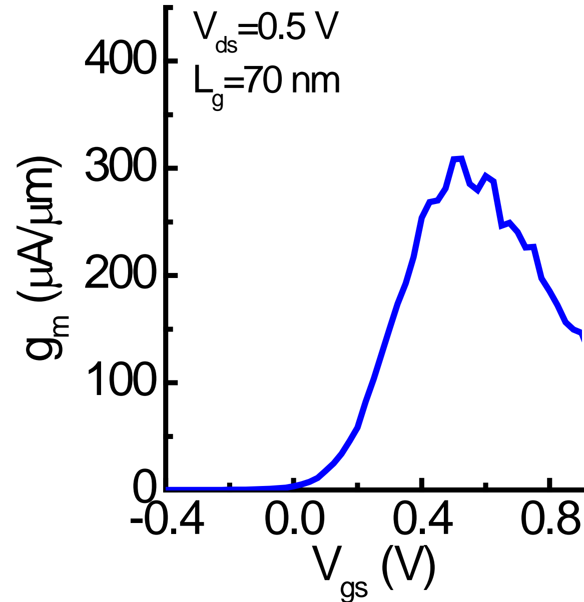


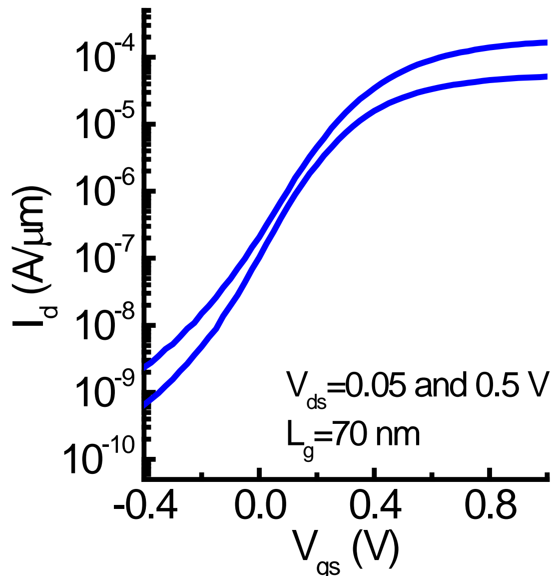


- **Process enables:**
  - Tight pitch: L_p=150 nm
  - Precise control of ledge: L_{ledge}=30 nm

Characteristics of L_g = 70 nm MOSFETs



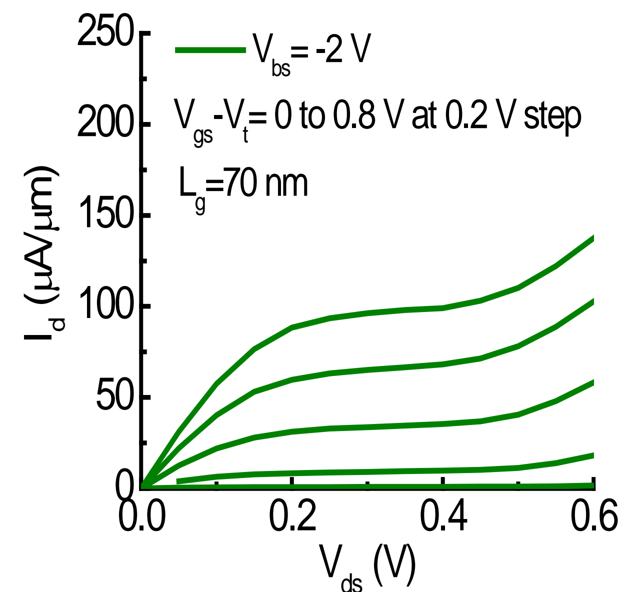


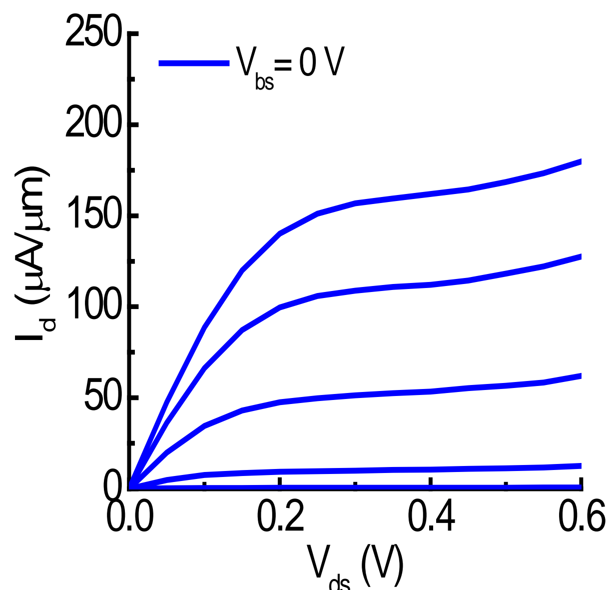


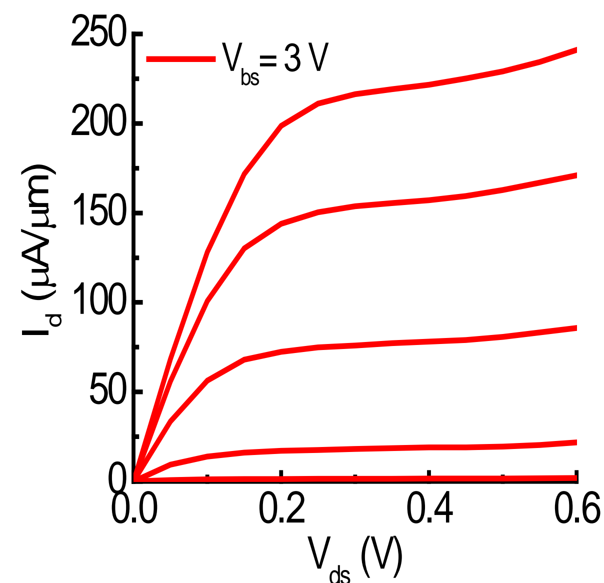
FOM at V_{ds}=0.5 V

- $g_{m,pk}$ = 309 µS/µm
- V_t = 96 mV
- S = 140 mV/dec
- DIBL = 80 mV/V
- R_{sd} = 1050 Ω.µm

Impact of Back Bias







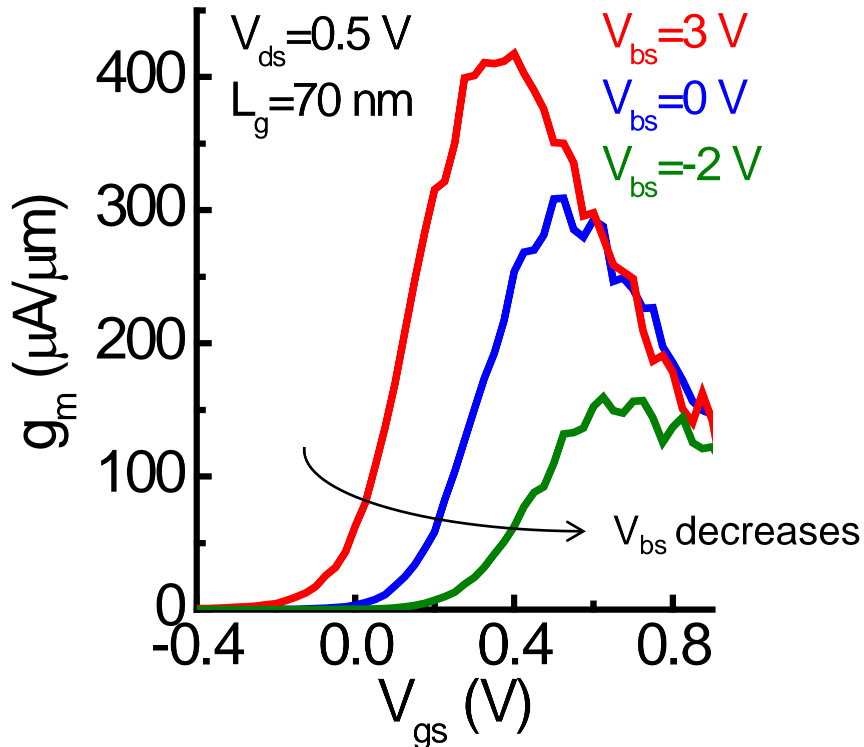
Positive V_{bs}:

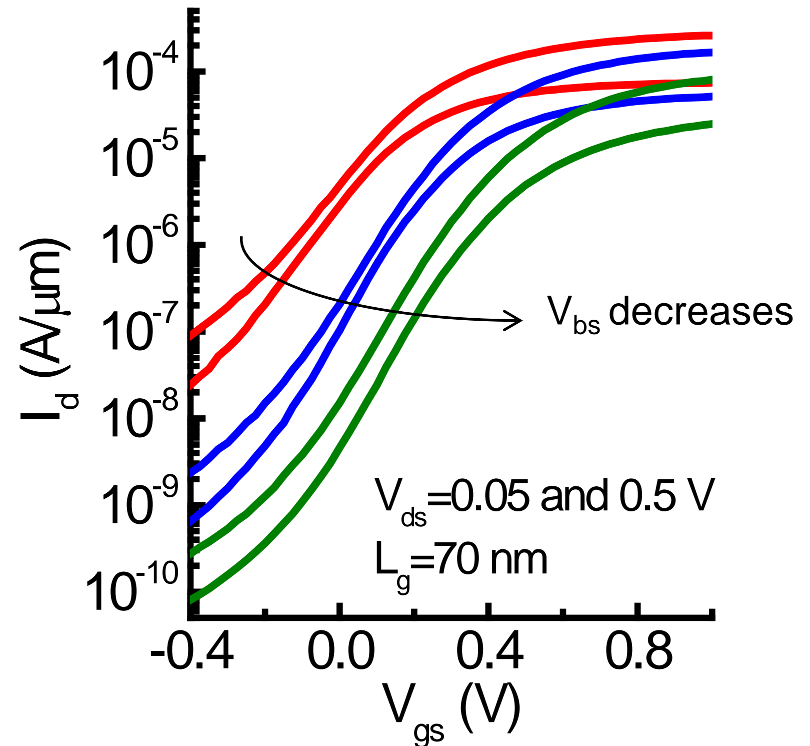
→ R_{on} ↓

→ I_d ↑

→ Output conductance↓

Impact of Back Bias



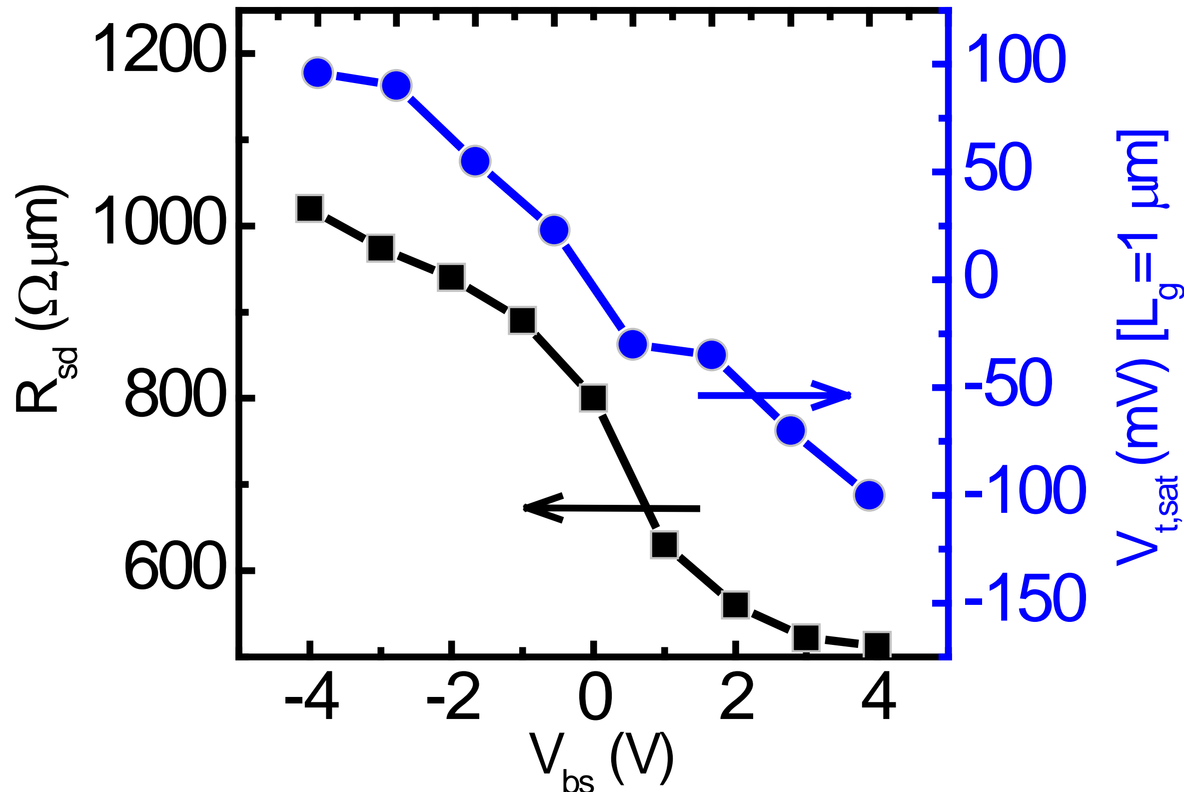


Positive V_{bs}:

$\rightarrow V_t \downarrow$ $\quad$ $\rightarrow$ S $\uparrow$

$\rightarrow g_m \uparrow$ $\quad$ $\rightarrow$ DIBL $\downarrow$

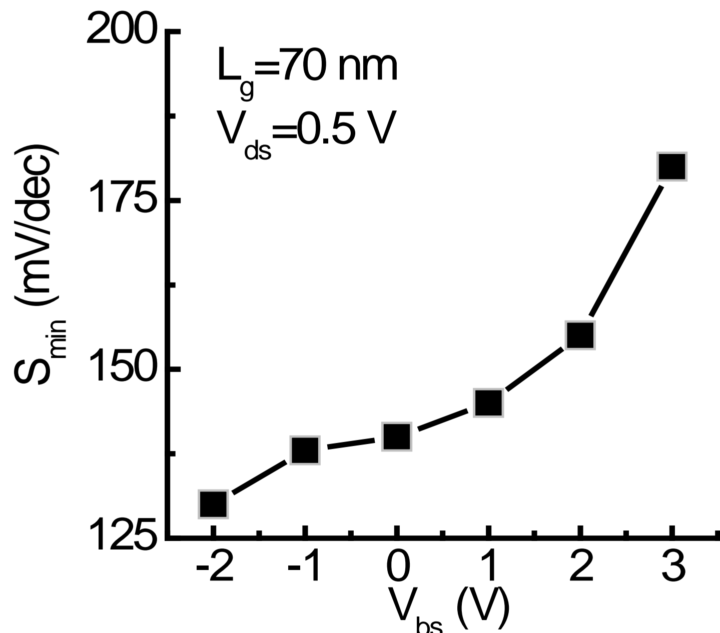
Impact of Back Bias on V_t and R_{sd}

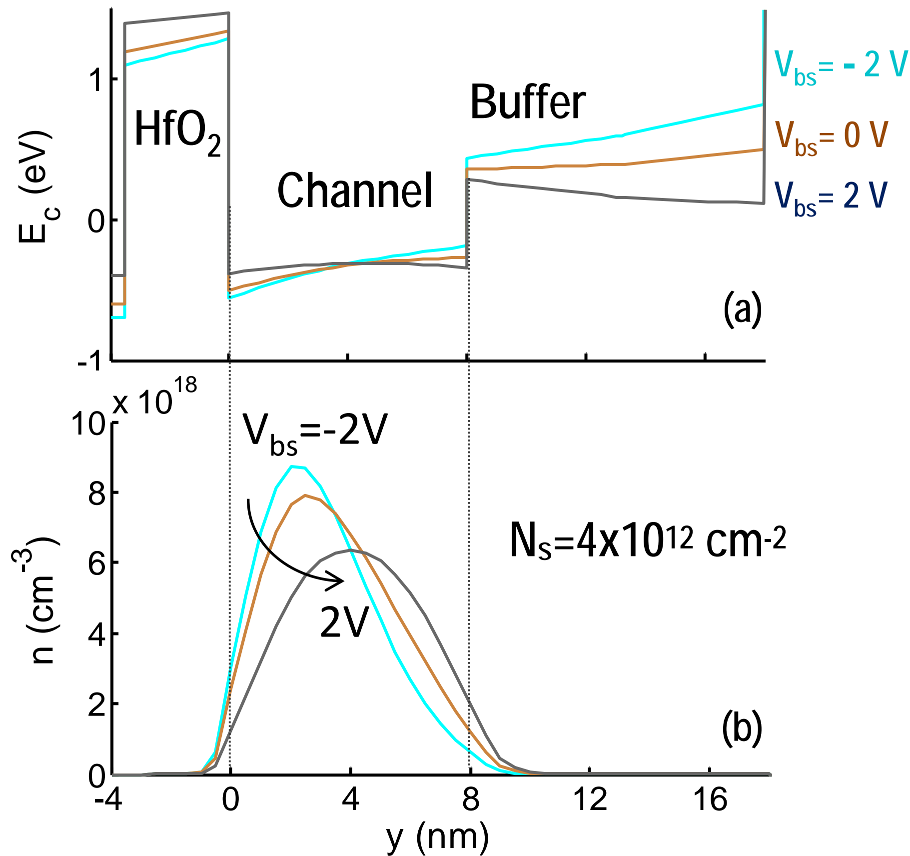


- R_{sd} modulation
- V_t tunability: ΔV_t= 200 mV for ΔV_{bs}= =±4 V

Impact of Back Bias on Subthreshold Swing

Poisson-Schrödinger simulation

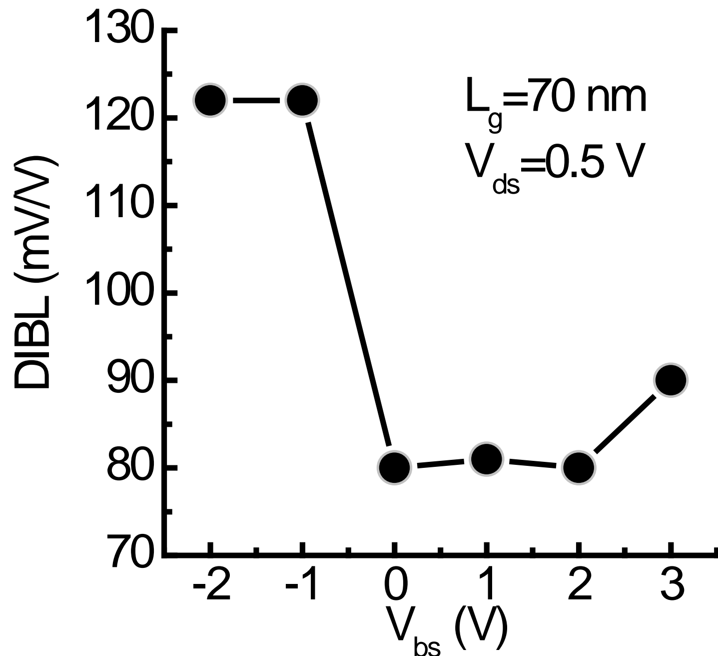




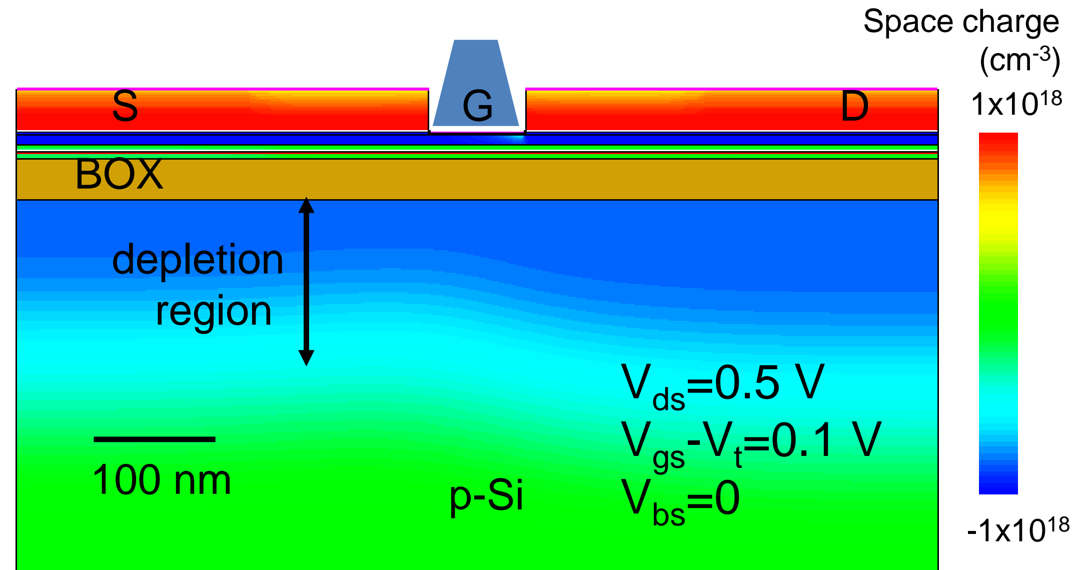
Positive V_{bs}
→ S ↑

Positive V_{bs}
→ Deeper electron centroid in channel

Impact of Back Bias on DIBL



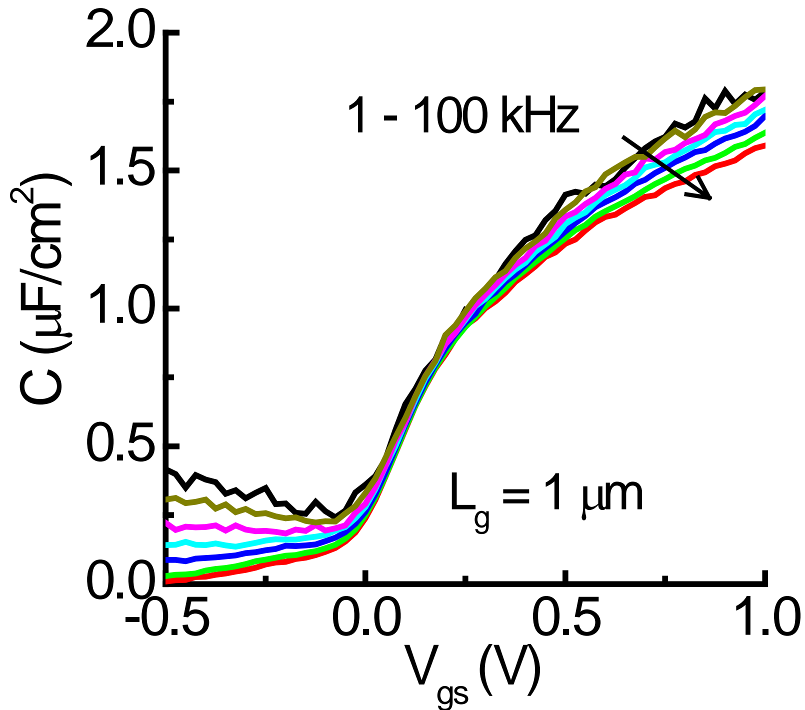
TCAD simulation of space charge

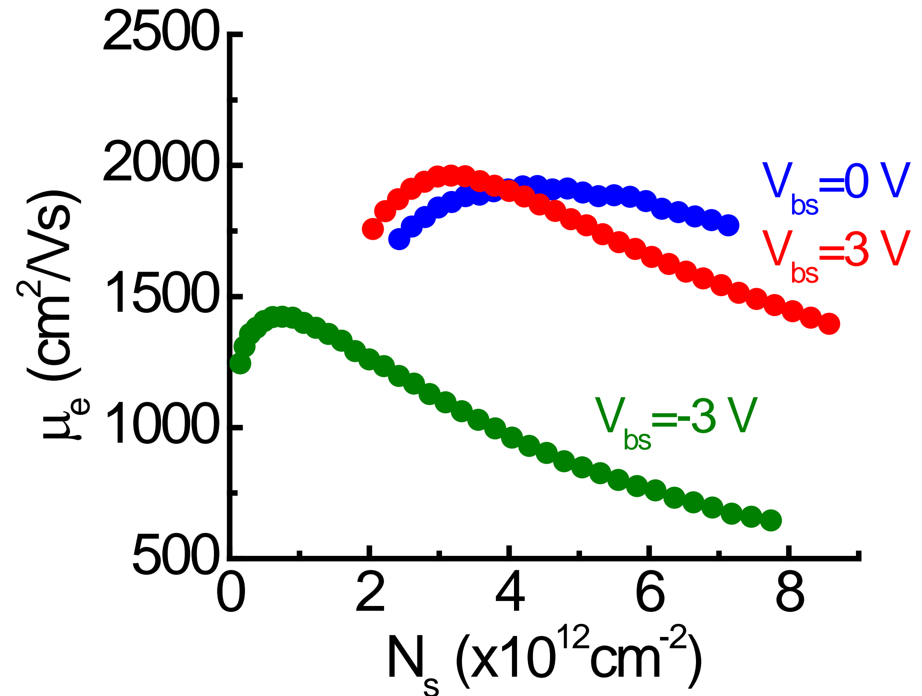


Positive V_{bs}
→ DIBL ↓

Positive V_{bs}
→ Si space charge region shrinks
→ Ground plane moves closer to channel

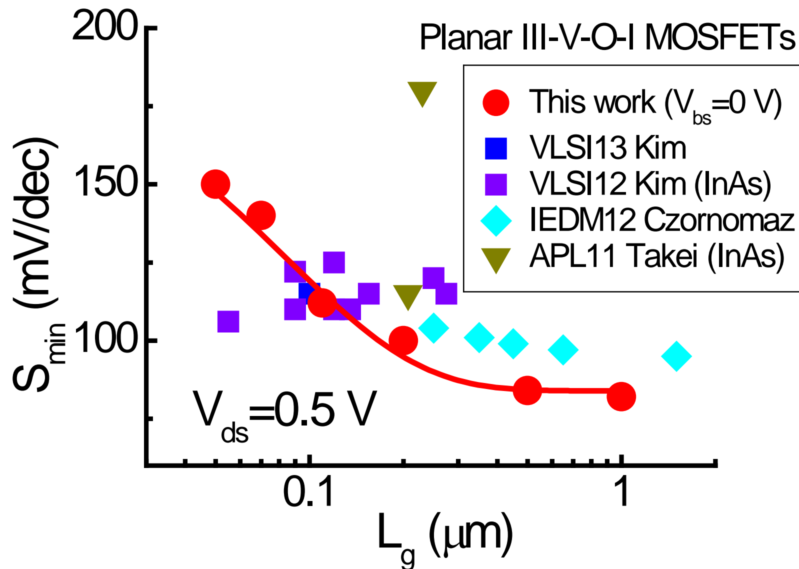
CV and Mobility

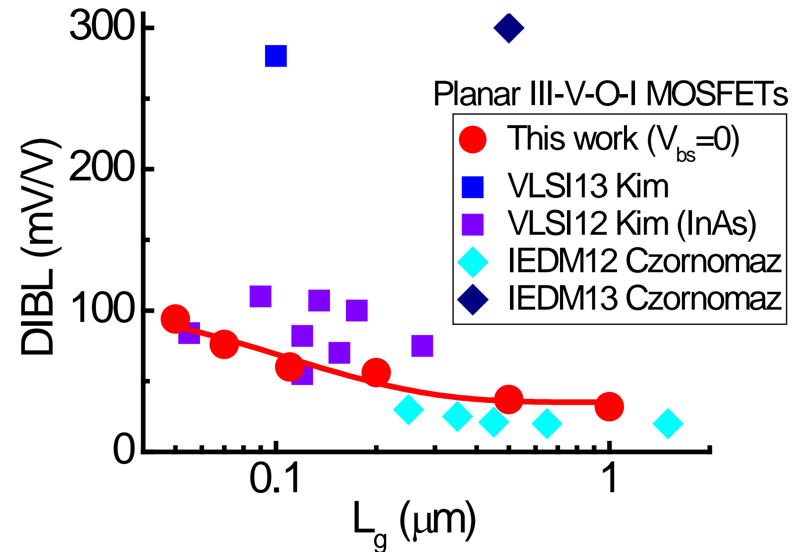


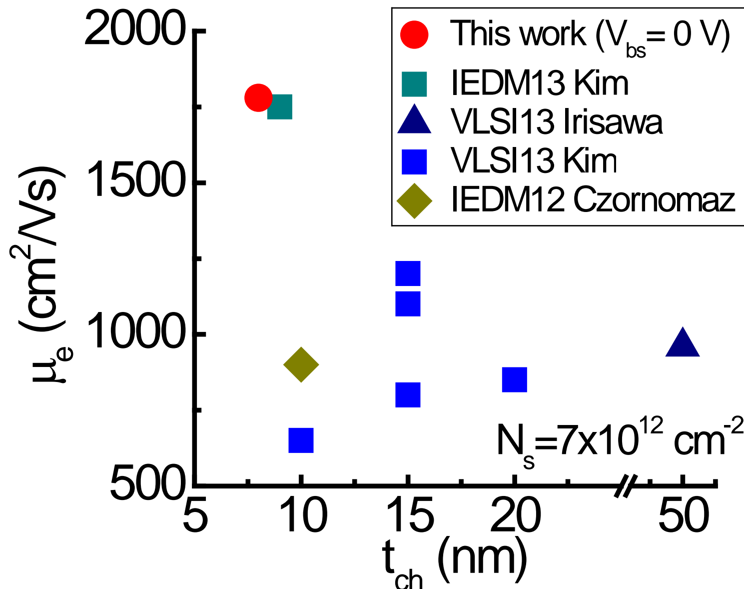


- Low frequency dispersion, CET~ 2 nm
- Lower mobility for negative V_{bs}
  → Confinement increases
- Front gate leakage < 10^{-3} A/cm^2 at V_g=1 V

Benchmarking of S, DIBL and Mobility







- Excellent S, DIBL and transport properties

Conclusions

- Demonstrated self-aligned $In_{0.7}Ga_{0.3}As$ MOSFETs on III-V-O-I on p-type silicon substrate
- Promising performance, need to lower R_{sd}
- Back gate bias allows wide tunability of device characteristics